ASP: An Aerospace Specification Process for Hardware Logic

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Abstract. This work intends to specify a process to develop aerospace devices that use VHDL (Very High-Speed Integrated Circuit (VHSIC) Hardware Description Language) to describe the digital hardware logic and assure all safety-critical features involved in the process were assessed. This work aims to a process that goes from the requirements to the logic implementation at the component described level. The research methodology contains 4 phases (Phases 1 to 4). We have already completed Phases 1 and 2. Currently, we are working on Phase 3. This work is being developed as part of a master's degree to be concluded by the end of 2023 inside of the Postgraduate Program in Space Sciences and Technologies of the Instituto Tecnológico de Aeronáutica.

Keywords: Aerospace, FPGA, VHDL, Requirements, life-cycle

1. Introduction

The use of complex electronic devices in safety-critical aerospace missions generates new safety and certification challenges. Complex electronic devices englobe programmable complex integrated circuits (IC) that can be programmed with logic inside. In addition, with the increased complexity, the possibility of incorrect logic or unexpected behavior is more likely [1-2]. To overcome the challenges of developing complex devices is necessary to ensure that errors are addressed in a more consistent and verifiable manner throughout the life cycle [1-2]. And requirements engineering allows to track that the developed hardware meets comply with the safety-critical aerospace device nature.

This work proposes a specification process to define the requirements that are singular, feasible, unambiguous, complete, consistent, verifiable, and traceable. Consequently, the requirements document will be used to develop aerospace digital hardware devices using VHDL. The rest of this work is organized as follows: Section 2 gives the review of the literature. Section 3 describes the research methodology. Section 4 presents the proposed specification process. Section 5 expresses the next steps of the research. Section 6 presents the final considerations.

2. Literature Review

In this section, we will describe standards and regulations that concern the development of aerospace devices.

2.1. Hardware Description Language

Hardware description languages such as VHDL can describe digital logic circuits and be synthesized in programmable logic devices (PLD). Hardware description language as the name implies describes the hardware. Therefore, digital circuit devices primarily work concurrently as physical hardware. This hardware perspective demands a different approach when writing a VHDL.

The VHDL code relies on synthesis tools to convert the code into logic cells from the target technology. The synthesis tools can only perform transformation and local optimization, and cannot convert a poor description into an efficient implementation, if the initial description is poor, the good configurations will be far away [11].

The IEEE 1076.6 [12] defines descriptions that can be portable between synthesis tools and how the semantics shall be used. It is important due to some VHDL structures cannot be synthesized. This work will deliver a good manner of writing a VHDL code, based on requirements, that can be easily readable and synthesized aiming to minimize the size of the circuit and meet the timing constraint.

Throughout the life cycle, this work intends to deliver ways to verify that each phase of development is correct and complete. The process is proactive to detect, record, evaluate, approve, track, and resolve deviations from approved plans and procedures to eliminate potential problems.

2.2. Requirements Engineering

The main point in any aerospace device is what it has to perform and discovering it in the early stages of development is a challenge addressed to requirements engineering [7]. According to IEEE 29148 [5], *Requirements engineering is concerned with discovering, eliciting, developing, analyzing, verifying (including verification methods and strategy), validating, communicating, documenting, and managing requirements* [5, 6].

This work is intended to deliver a comprehensive view of how to use the tools that requirements engineering has to offer. Tracking the customer needs and then writing documents in a manner that we could analyze if feasible, and verify what the customer wants to be done.

To discover what the customer wants or thinks he wants there are many techniques to conduct requirements elicitation such as brainstorming, card sorting, interviews, prototyping, use cases, user stories, etc. Choosing one elicitation technique for a specific domain is a challenge [6]. There are many forms to represent requirements, from natural language, visual models, and formal methods. Proper representations facilitate communication with all involved.

Requirements can be categorized into functional and non-functional requirements. Where functional requirements (FRs) can define what the device should provide and how the device will react to its inputs such as data manipulation [4]. In essence, it’s a product feature and delivers what the device should do. Non-functional requirements (NFRs) can be defined as how the device should behave concerning some attributes such as reliability, reusability, maintainability, and security. Generally, any attribute or quality that ends in “ility” is an NFR [4, 8]. By its nature, FRs are easier than NFRs to capture and document. Despite the nature of NFRs being hard to capture, reports reveal that neglecting them can lead to catastrophic project failures, or at the very least, to delays and consequently rises in the final cost [4, 8]. Aerospace devices are safety-critical, thus, during the elicitation of the requirements, special attention must be dedicated to discovering and categorizing all the NFRs related to safety issues. Thus, to facilitate the process of development of the VHDL components, where the described component is a mere translation from the requirements to VHDL code and can be assessed against the elicited requirements.

2.3. ECSS-E-ST-10-06C - Space Engineering - Technical Requirements Specification

This standard is one of the series of ECSS (European Cooperation for Space Standardization), requirements in this standard are defined in terms of what shall be achieved. This standard delivers an overview of the technical requirements specification, and it is applicable to all types of space systems, all product elements, and projects. The standard delivers a process for establishing a technical requirements specification, with different phases and steps like identifying possible concepts, selecting possible concepts, enhancing the previous elicited requirements, categorizing and justifying, and assessing for correctness, and consistency [7].

2.4. IEEE 29148 - Systems and Software Engineering - Life Cycle Process - Requirements Engineering

The IEEE 29148 [5] delivers a model that the final result is a document called SRS (System Requirements Specification) that helps to establish the agreement between all personnel involved, force a rigorous assessment of requirements before implementation, one key point about IEEE 29148 is this standard has been widely deployed in several applications domains [4]. IEEE 29148 provides guidance to deal with functional and non-functional requirements.

3. Research Methodology

The methodology contains 4 phases to conduct this master’s degree work. Phase 1 involves the identification of our Research Questions. The second phase (Phase 2) requires the literature review of related works and the standards involved. Phase 3 focuses on the definition of our main contribution, the Aerospace Specification Process (ASP) for Hardware Logic. Phase 4 will evaluate the ASP. Figure 1 presents the methodology phases. Our Research Questions (RQs) are presented in Table 1.

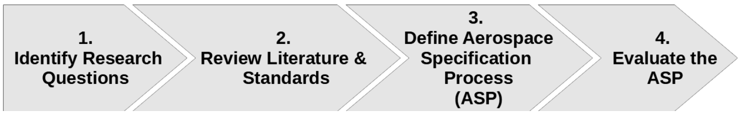
1.
Identify Research Questions
2.
Review Literature & Standards
3.
Define Aerospace Specification Process (ASP)
4.
Evaluate the ASP

Fig. 1. Methodology Phases

Tab. 1. Research Questions

ID	Research Question	Justification
RQ1	How to properly specify and validate aerospace hardware requirements for logic devices to ensure they are singular, feasible, unambiguous, complete, consistent, verifiable, and traceable?	The requirements correctness must be ensured by the use of the specification process defined by this master's research.
RQ2	How to satisfy standards to be used for hardware logic for Aerospace applications?	Standards are claimed by contracts or in some cases if certification is required. Thus the satisfaction of standards will enrich the specification process to be developed as part of this work.

4. Aerospace Specification Process (ASP)

The requirements identification in the early stage of development helps the selection of the right technology to be used, what hardware should be selected, and what standards and regulations should be applied [8]. The specification process guides how to prepare a requirement document detailing all the steps and the respective outputs of each step. For this task, this work will rely on trustworthy standards and guides, combining them to obtain a document that suits the development of an aerospace device using VHDL (Fig. 2). The first step is to extract from customers a preliminary requirement document called PDRS (Preliminary Device Requirements Specification). Figure 3 depicts a design flow proposed to obtain a PDRS.

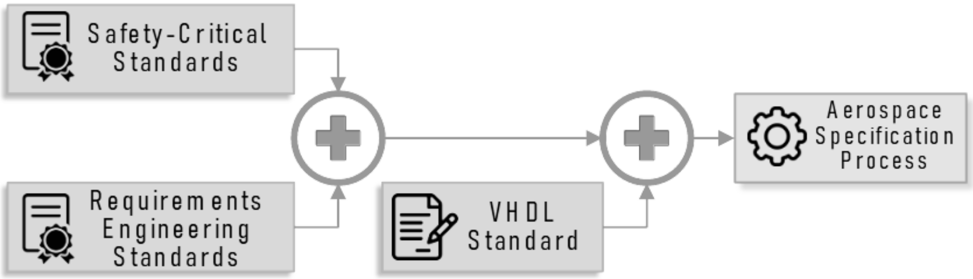
Safety-Critical Standards
Requirements Engineering Standards
VHDL Standard
Aerospace Specification Process

Fig. 2. Aerospace Specification Proces (ASP) sequence.

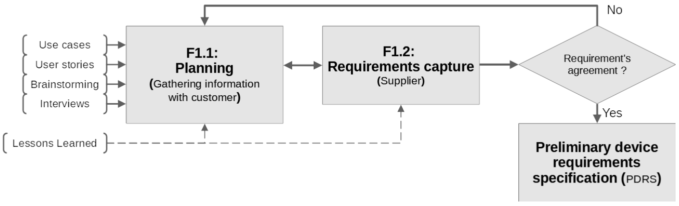
No
Use cases
User stories
Brainstorming
Interviews
F1.1:
Planning
(Gathering information with customer)
F1.2:
Requirements capture
(Supplier)
Requirement's agreement ?
Yes
Lessons Learned
Preliminary device requirements specification (PDRS)

Fig. 3. Tasks to be completed in order to obtain a PDRS.

The **F1.1 planning** step (Fig. 3) shall collect information by elicitation techniques with all personnel involved like external devices connected with the device in development such as memories, buses, etc. In addition, discover what laws regulate where the developed device will operate.

The next step, **F1.2 requirements capture** (Fig. 3) is where the supplier (requirements engineer) will write the document with the information collected from the planning step F1.1. The requirements should state "what-is-necessary", as opposed to telling the supplier "how-to". Unless the task demands ensuring the proper functions of the developed device. The structure of requirements written shall be a complete sentence, with a verb and a noun, always in a positive way [7].

After the requirements engineer has written the draft document of requirements there is a step of agreement (Fig. 3), where the parts interested agree with the **preliminary device requirements specification** (PDRS). It is important to mention these first steps are the time to bring consensus to discussions, test hypotheses, exhaust the theme, and address dramatic changes.

Figure 4 shows the next steps toward a consolidated Device Requirements Specification (DRS).

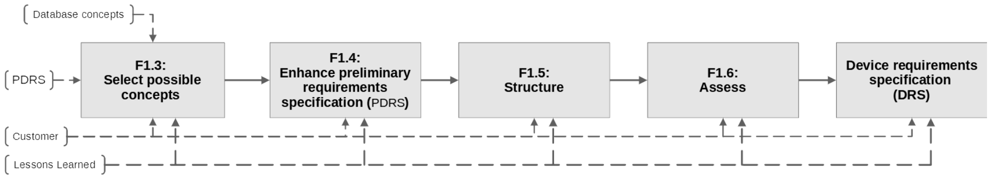

Fig. 4. The steps to produce an assertive device requirements specification (DRS).

The first step, **F1.3 Selecting possible concepts** (Fig. 4), is used to create a high-level block diagram that suits the information collected in PDRS. At this point, with the customer's intervention, a feasible solution is chosen for the device specified in PDRS.

The next step, **F1.4 Enhance PDRS** (Fig. 4), with new information collected with a high-level block diagram and taking into account the limitations and possibilities induced by the selected concept. The PDRS is updated.

Finally, it is important to note, that this is an evolutionary model, where if new changes need to be added, the flow of development is not supposed to suffer drastic changes. Because at every step there is an opportunity to evaluate the process.

Figure 5 depicts a low-level block representation, related to step **F1.5 Structure** (Fig. 4); The FPGA block contains the components to be written in VHDL to connect the FPGA with the external components.

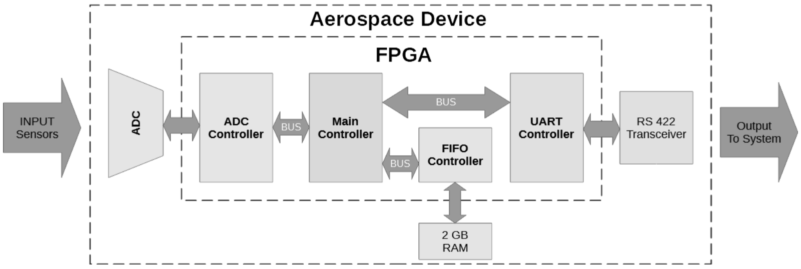

Fig. 5. Proposed VHDL blocks.

In the next step, **F1.6 Assess** (Fig. 4), at this stage, the DRS document is almost complete, however, a final round of discussion with all personnel involved is required. It is fundamental the encouragement for all to speak their opinions. Any minor change must be assessed. After the agreement, the final step, Device Requirements Specification (DRS) is generated.

5. Next Steps

Firstly, the task of detailing the specification process and mitigating any deficiencies. Many of the failures or problems involving FPGA devices in aerospace applications are due to inadequate development processes [9]. Currently, we have finished Phases 1 and 2. Phase 3 is started, as presented in Section 4.

To improve Phase 3, we plan an approach using the instructions provided by the standards and additional information obtained from the related works developed in safety-critical areas, such as nuclear power plants. Therefore, studying how these standards and correlated works deal with safety-critical problems, thus understanding their similarities and differences. Thus, compiling a new process that has been modified and enhanced to reflect what is required to specify a VHDL logic for the aerospace devices.

As soon as we finish Phase 3, we plan to conduct Phase 4, with the evaluation of ASP. We will conduct one experiment to exercise our process, and we will also plan to conduct a focal group with aerospace experts from Instituto de Aeronáutica e Espaço (IAE), Instituto Nacional de Pesquisas Espaciais (INPE) and Instituto Tecnológico de Aeronáutica (ITA) for independent evaluation of ASP. During Phase 4, the correctness and satisfaction of the requirements of related standards will also be evaluated to ensure RQ1 and RQ2 were answered.

6. Final Considerations

With this work, we intend to specify a process of development for aerospace devices that operate with FPGA, and use VHDL as a programming language. The specified process will describe the required hardware that will perform in a safety-critical environment the behavior as described by the collected requirements.

As depicted in Figure 2, the process to achieve the goal of this work is presented in 4 phases. The first and second phases have been finished, where research questions and systematic literature and standards review has been done. We have searched in a database of renowned airspace agencies like NASA, ESA, and FAA for documents, standards, handbooks, and application notes that would help us to respond to the questions of phase 1. Scientific articles also were included in the task of review of the literature. Moreover, the third phase (phase 3) is still in motion. In phase 3 an effort is made toward defining the ASP. At this point, a study is being conducted on how the similarities and differences found in the review of the literature would help to develop a consolidated answer for the research questions. Thus, creating aerospace devices that are described in VHDL and synthesized in FPGAs that would operate with no further concerns in safety-critical environments.

Finally, after phase 3 is finished with success, phase 4 will begin. In phase 4, we intend to evaluate the ASP by putting it against an experiment to exercise the process. We plan that the result of this exercise will be analyzed by a focal group of aerospace experts. Thus, receiving feedback on the proposed process from experts. In conclusion, at the end of this phase, the research questions proposed in phase 1 shall be answered and the ASP validated.

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